REMARKS/ARGUMENTS

Favorable reconsideration of this application is respectfully requested.

Claims 16-33 are pending in this application. Claims 16-33 were rejected under 35 U.S.C. §103(a) as unpatentable over applicant's admitted art of Figure 1 in view of U.S. patent 5,553,200 to Accad and U.S. patent 5,864,652 to Murahashi.

Addressing the above-noted rejection, that rejection is traversed by the present response.

Initially, applicant notes the claims are amended by the present response to clarify features recited therein. Specifically, independent claim 16 now further recites "the second memory is connected to the image data processing unit, not via the unit". According to such a claimed feature, and with reference to Figure 15 in the present specification as a non-limiting example, a second memory 107 is connected to an image data processing unit 108, not via an interfacing unit 103. Stated another way, in the claimed invention the second memory 107 is not directly connected to the interface unit 103 and does not need the interface unit 103 for connection to the processing unit 108. The other independent claims are amended to recite similar features, claims 28-33 reciting the second image data memory "directly" connected to the image data processing unit.

With respect to Figure 15 in the present specification as a non-limiting example, an image data processing unit 108 includes a graphics port 106 and a peripheral device interconnection port 109, the peripheral device interconnection port 109 configured to be connected to a print engine 110. Further, a first image data memory 104 and a second image data memory 107 are provided. A unit 103, shown in Figure 2 as a North Bridge (NB), is connected to the graphics port 106 of the image data processing unit 108 and has a function to interface between the image data processing unit 108 and the first image data memory 104. Further, the first image data memory 104 is connected to the image data processing unit 108

via the unit 103. The second image data memory 107 is connected to the image data processing unit 108 not through the unit 103.

Compressed image data is controlled to be transferred from the first image data memory 104 to the second image data memory 107, and then from the second image data memory 107 to the image data processing unit 108. The image data processing unit 108 decompresses the transferred compressed image data and outputs the decompressed image data to the print engine 110.

The basis for the outstanding rejection recognizes that the admitted art of Figure 1 does not teach the claimed "unit". To overcome that deficiency in the admitted art the outstanding Office Action cites Accad, and specifically references the chipset 405 including a DMA 406. In supporting the outstanding rejection the outstanding Office Action states:

> It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of Accad into the system of APA in order to provide central control of the devices which connected to the bus bridge because a bus bridge or chip set controls the system and its capabilities. It is the ***hub of all data transfer***.[1]

In Figure 4 Accad discloses a controller chipset 405 to which all elements are connected. Incorporating such teachings of Accad into the admitted art would not realize the claimed invention.

As clarified in the claims, in the claimed invention the second memory is connected to the image data processing unit, not via the unit. Again with reference to Figure 15 in the present specification as a non-limiting example, the second memory 107 is not connected to the north bridge interface unit 103, but instead is connected to the image data processing unit 108.

The above-noted basis for the outstanding rejection relies upon the controller chipset 405 in Accad as being "the hub of ***all data transfer***" (emphasis added). Thereby, if the

[1] Office Action of May 23, 2006, top of page 3 (emphasis added).

teachings in Accad were combined with the teachings of the admitted art of Figure 1, that would result in all data transfer being routed through a type of central controller chipset interface. The claims require a different operation as in the claims the second memory is not connected to such a central interface. Thereby, the claims distinguish over the applied art.

Stated another way, if the teachings of Figure 4 in Accad were combined with the admitted art of Figure 1 that would result in all the memory units, including the memories 1605 and 1608 of Figure 1, to be connected to such a central controller chipset. The claims require a different structure.

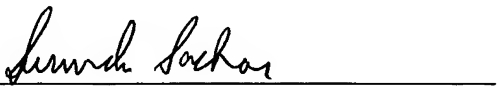
With respect to independent claims 30 and 31, no combination of teachings of the admitted art, Accad, and Murahashi disclose the further recited feature that the decompressed image data is output from the image data processing unit "in accordance with an output timing to output the decompressed image data to the print engine".

In view of these foregoing comments, the claims as currently written are believed to clearly distinguish over the applied art.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Gregory J. Maier
Attorney of Record
Registration No. 25,599

Surinder Sachar
Registration No. 34,423

Customer Number
22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 03/06)
SNS/rac
I:\ATTY\SNS\22'S\220449\220449US-AM3.DOC